

**WHAT IS CLAIMED IS:**

1. A semiconductor memory device comprising:

a word line;

a first bit line intersecting with the word line;

5 a second bit line forming a bit line pair with the first bit line;

a memory cell including an access transistor of an MISFET in which a gate electrode is connected to the word line and a first doped layer is connected to the first bit line, and a cell capacitor connected to a second doped layer of the access transistor, being capable of storing electric charge, and located at the intersection between the word line and

10 the first bit line; and

a sense amplifier for amplifying a potential difference between the first bit line and the second bit line during a read-out operation

wherein a positive power supply voltage is applied to the first bit line in a high level state and a ground voltage is applied to the first bit line in a low level state,

15 wherein the access transistor is a depletion type p-channel MISFET, and

wherein the ground voltage is applied to a gate electrode of the access transistor through the word line when the memory cell is in an activated state.

2. The semiconductor memory device of claim 1, wherein an increased potential  
20 higher than the positive power supply voltage is applied to the gate electrode of the access transistor in a non-activated state.

3. The semiconductor memory device of claim 1, wherein the cell capacitor is a p-channel MISFET.

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4. The semiconductor memory device of claim 3, wherein the cell capacitor is a planar type MISFET.

5. The semiconductor memory device of claim 3, wherein the cell capacitor is a  
5 depletion type MISFET, and

wherein during an operation period, the ground voltage is applied to the gate electrode of the cell capacitor.

6. The semiconductor memory device of claim 1, wherein the access transistor and  
10 the cell capacitor share a substrate or an n-type well to which the positive power supply voltage is applied.

7. The semiconductor memory device of claim 1, wherein the sense amplifier includes:

15 an amplifier circuit which includes a pair of p-channel MISFETs and amplifies a potential difference between the pair of bit lines; and

a p-channel drive MIS transistor which controls driving of the amplifier circuit and has a lower threshold voltage than that of the pair of p-channel MISFETs.

20 8. The semiconductor memory device of claim 7, wherein each of the pair of p-channel MISFETs is a depletion type MISFET.

9. The semiconductor memory device of claim 1, further comprising a precharging/equalizing circuit including:

25 a bit line equalizing transistor of a depletion type p-channel MISFET for short-

circuitting between the first bit line and the second bit line during a period in which the memory cell is in a non-activated state;

a bit line precharging transistor of depletion type p-channel MISFET for applying a constant voltage to the bit line pair during a period in which the memory cell is in a non-activated state.

10. The semiconductor memory device of claim 9, wherein a voltage higher than a threshold voltage is applied to each gate electrode of the bit line equalizing transistor and the bit line precharging transistor during a period in which the memory cell is in a non-activated state.

11. The semiconductor memory device of claim 9, wherein the access transistor, the bit line equalizing transistor, the bit line precharging transistor and the pair of p-channel MISFETs in the sense amplifier are formed in a common process step.

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12. A semiconductor memory device comprising:

a word line;

a first bit line intersecting with the word line;

a second bit line forming a bit line pair with the first bit line;

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a memory cell including an access transistor of an MISFET in which a gate electrode is connected to the word line and a first doped layer is connected to the first bit line, and a cell capacitor connected to a second doped layer of the access transistor, being capable of storing electric charge, and located at the intersection between the word line and the first bit line; and

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a sense amplifier for amplifying a potential difference between the first bit line and

the second bit line during a read-out operation

wherein a positive power supply voltage is applied to the first bit line in a high level state and a ground voltage is applied to the first bit line in a low level state,

wherein the access transistor is a depletion type n-channel MISFET, and

5 wherein the positive voltage is applied to a gate electrode of the access transistor through the word line when the memory cell is in an activated state.

13. The semiconductor memory device of claim 12, wherein a negative increased potential lower than the ground voltage is applied to the gate electrode of the access  
10 transistor in a non-activated state.

14. The semiconductor memory device of claim 12, wherein the cell capacitor is an n-channel MISFET.

15 15. The semiconductor memory device of claim 12, wherein the sense amplifier includes:

an amplifier circuit which includes a pair of n-channel MISFETs and amplifies a potential difference between the pair of bit lines; and

an n-channel drive MIS transistor which controls driving of the amplifier circuit  
20 and has a higher threshold voltage than that of the pair of n-channel MISFETs.

16. A semiconductor integrated circuit device comprising:

a logic circuit which includes a p-channel MISFET and is integrated on a substrate;  
and

25 a dynamic semiconductor memory device provided on the substrate on which the

logic circuit is provided and including a word line, a first bit line intersecting with the word line, a second bit line forming a bit line pair with the first bit line, a memory cell including an access transistor of a p-channel MISFET in which a gate electrode is connected to the word line and a first doped layer is connected to the first bit line, and a cell capacitor  
5 connected to a second doped layer of the access transistor, being capable of storing electric charge, and located at the intersection between the word line and the first bit line, and a sense amplifier for amplifying a potential difference between the first bit line and the second bit line during a read-out operation

wherein the threshold voltage of the access transistor is set to be higher than that of  
10 the p-channel MISFET provided in the logic circuit.

17. The semiconductor integrated circuit device of claim 16, wherein the access transistor is a depletion type MISFET, and

wherein the ground voltage is applied to a gate electrode of the access transistor  
15 through the word line when the memory cell is in an activated state.

18. The semiconductor integrated circuit device of claim 16, wherein the cell capacitor is a p-channel MISFET.

20 19. The semiconductor integrated circuit device of claim 18, wherein the cell capacitor is a planar type MISFET.

20. The semiconductor integrated circuit device of claim 16, wherein the cell capacitor is a depletion type MISFET, and

25 wherein the ground voltage is applied to a gate electrode of the cell capacitor

during an operation period.

21. The semiconductor integrated circuit device of claim 17, wherein the access transistor includes a gate insulation film having a greater thickness than the thickness of a  
5 gate insulation film of the p-channel MISFET in the logic circuit.

22. The semiconductor integrated circuit device of claim 17, wherein the thickness of the gate insulation film of the access transistor is equal to the thickness of a gate insulation film of the cell capacitor.

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23. The semiconductor integrated circuit device of claim 16, wherein the access transistor and the cell capacitor share a substrate or an n-type well to which the positive power supply voltage is applied, and

wherein the positive power supply voltage is applied to the first bit line in a high  
15 level state and the ground voltage is applied to the first bit line in a low level state.

24. The semiconductor integrated circuit device of claim 16, wherein the sense amplifier includes:

an amplifier circuit which includes a pair of p-channel MISFETs and amplifies a  
20 potential difference between the pair of bit lines; and

a p-channel drive MIS transistor which controls driving of the amplifier circuit and has a lower threshold voltage than that of the pair of p-channel MISFETs.

25. The semiconductor integrated circuit device of claim 24, wherein each of the  
25 pair of p-channel MISFETs is a depletion type MISFET.

26. The semiconductor integrated circuit device of claim 24, wherein the dynamic semiconductor memory device further includes a precharging/equalizing circuit including:

5 a bit line equalizing transistor of a depletion type p-channel MISFET for short-circuiting between the first bit line and the second bit line during a period in which the memory cell is in a non-activated state; and

a bit line precharging transistor of a depletion type p-channel MISFET for applying a constant voltage to the bit line pair during a period in which the memory cell is in a non-activated state.

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27. The semiconductor integrated circuit device of claim 26, wherein a voltage higher than a threshold voltage is applied to each gate electrode of the bit line equalizing transistor and the bit line precharging transistor during a period in which the memory cell is in a non-activated state.

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28. The semiconductor integrated circuit device of claim 16, wherein the dynamic semiconductor memory device is formed by the same logic process used for the logic circuit.

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29. A semiconductor integrated circuit device comprising:

a logic circuit which includes a n-channel MISFET and is integrated on a substrate; and

a dynamic semiconductor memory device provided on the substrate on which the logic circuit is provided and including a word line, a first bit line intersecting with the word  
25 line, a second bit line forming a bit line pair with the first bit line, a memory cell including

an access transistor of an n-channel MISFET in which a gate electrode is connected to the word line and a first doped layer is connected to the first bit line, and a cell capacitor connected to a second doped layer of the access transistor, being capable of storing electric charge, and located at the intersection between the word line and the first bit line, and a  
5 sense amplifier for amplifying a potential difference between the first bit line and the second bit line during a read-out operation

wherein the threshold voltage of the access transistor is set to be lower than the threshold voltage of the n-channel MISFET provided in the logic circuit.

10 30. The semiconductor integrated circuit device of claim 29, wherein the access transistor is a depletion type MISFET, and

wherein a positive power supply voltage is applied to a gate electrode of the access transistor through the word line when the memory cell is in an activated state.

15 31. The semiconductor integrated circuit device of claim 29, wherein the cell capacitor is an n-channel MISFET.

32. The semiconductor integrated circuit device of claim 29, wherein the sense amplifier includes:

20 an amplifier circuit which includes a pair of n-channel MISFETs and amplifies a potential difference between the pair of bit lines; and

an n-channel drive MIS transistor which controls driving of the amplifier circuit and has a higher threshold voltage than that of the pair of n-channel MISFETs.